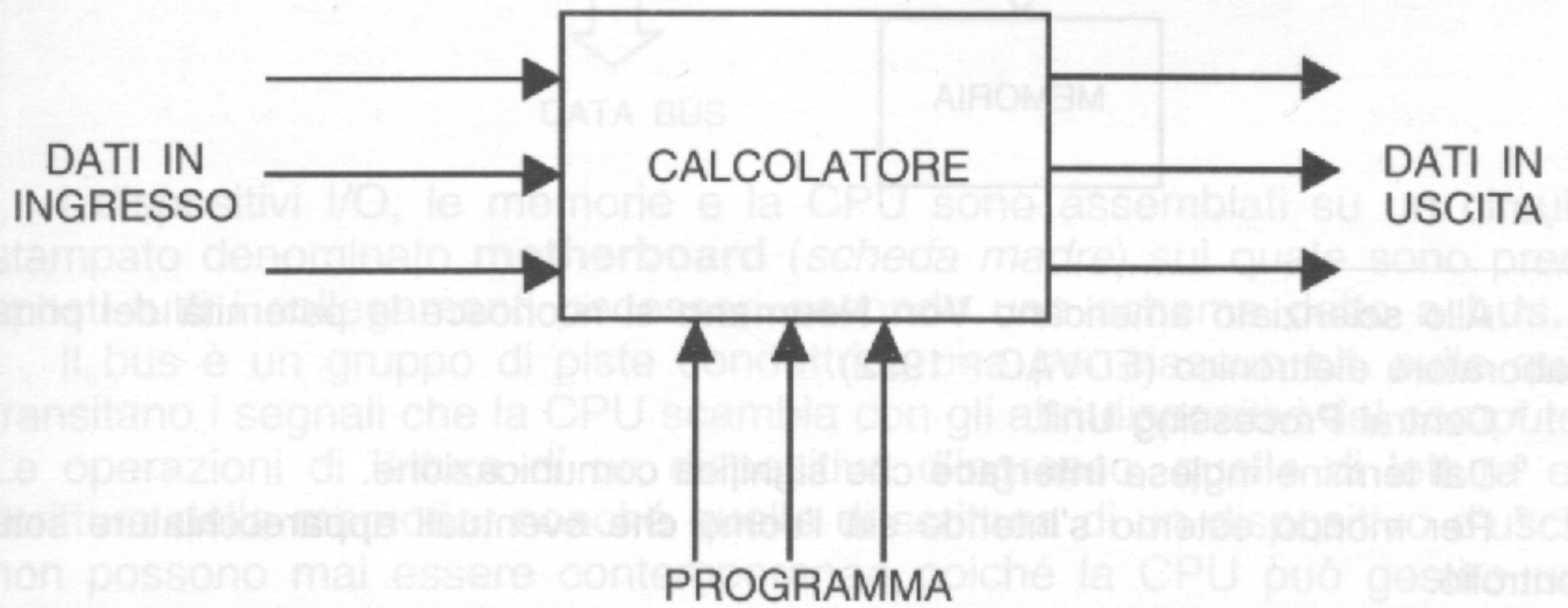

DATI IN
INGRESSO
CALCOLATORE
DATI IN
USCITA
PROGRAMMA

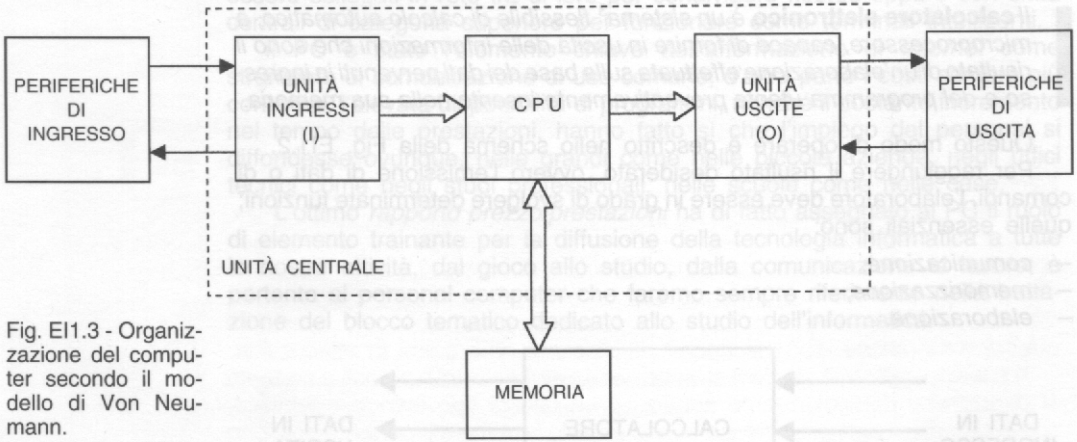
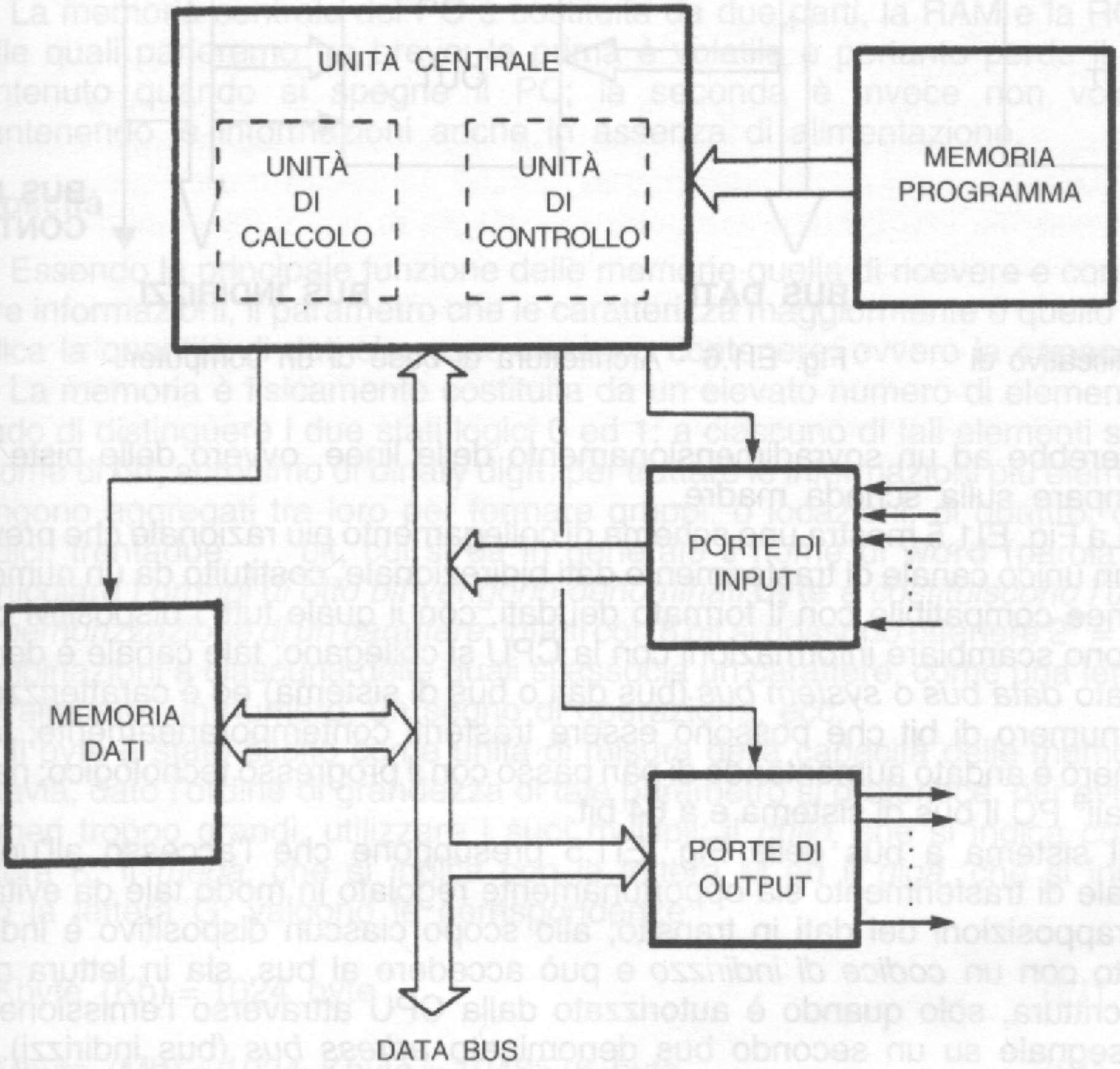
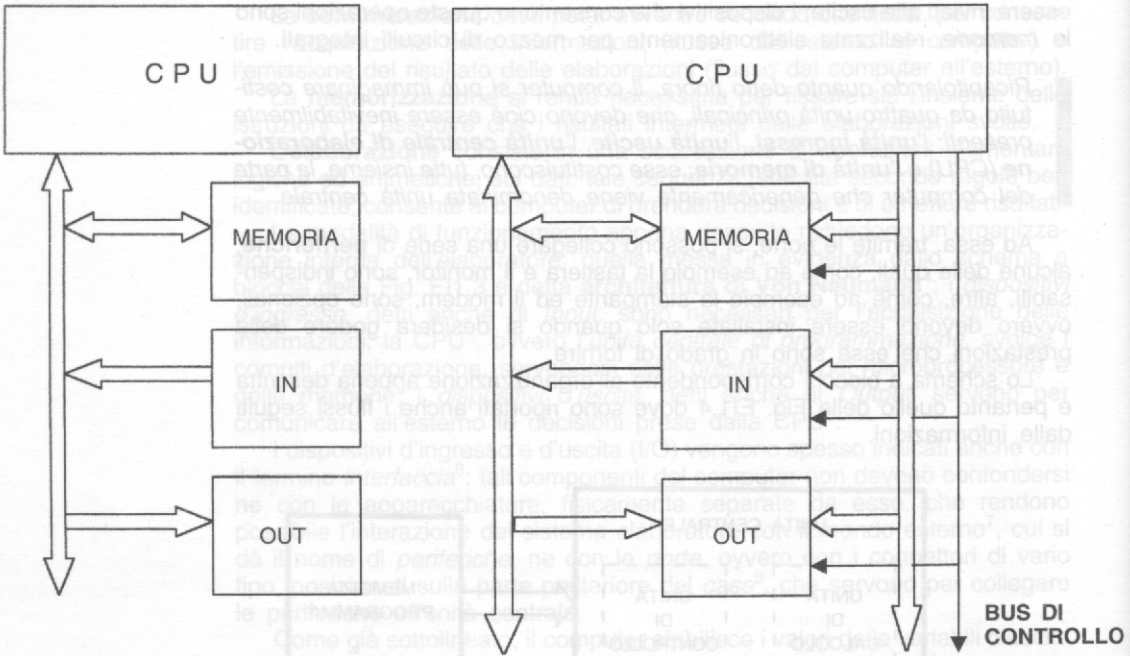
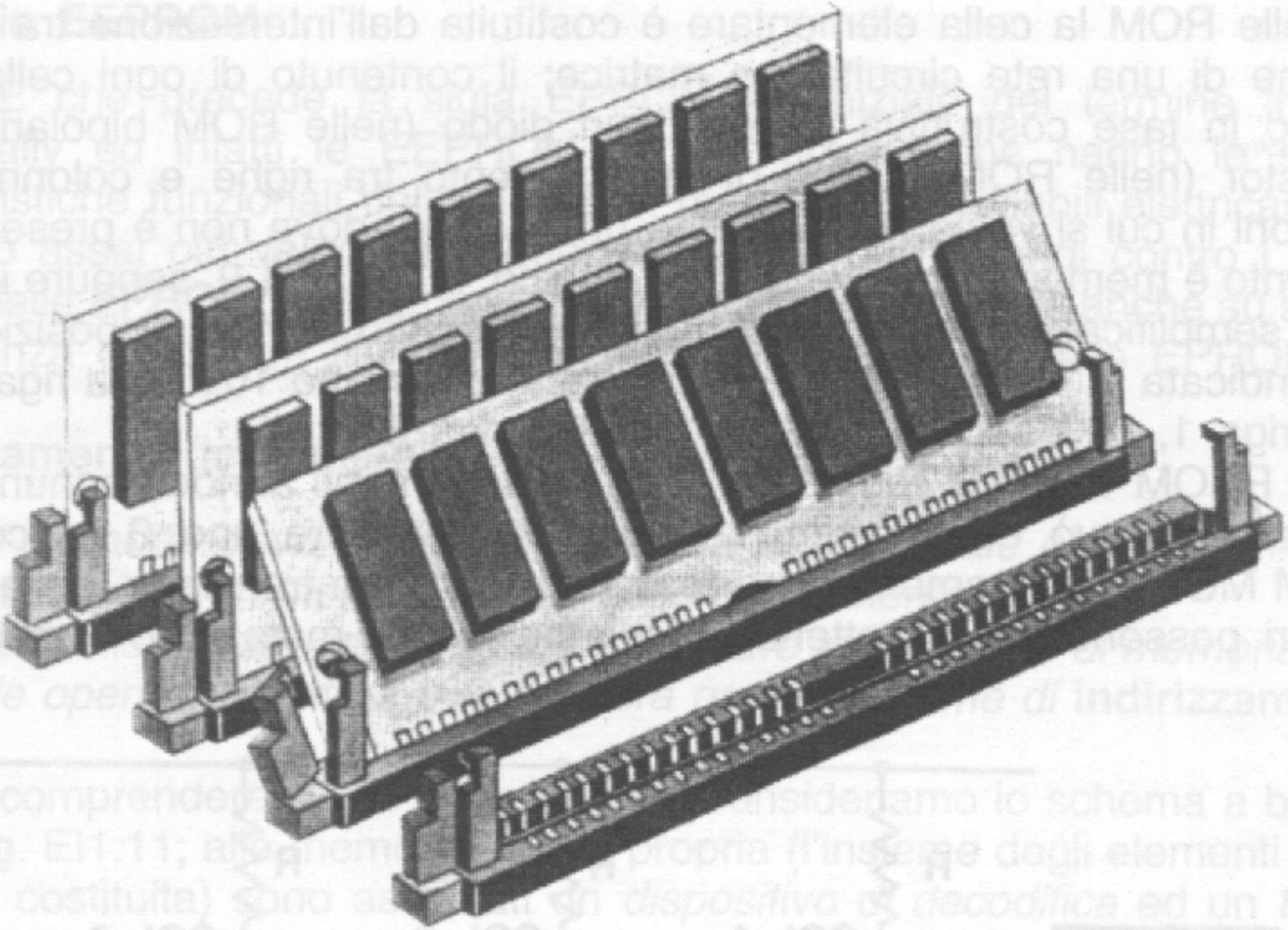


Fig. EI1.3 - Organizzazione del computer secondo il modello di Von Neumann.


UNITÀ CENTRALE
UNITÀ DI CALCOLO
UNITÀ DI CONTROLLO
MEMORIA PROGRAMMA
PORTE DI INPUT
MEMORIA DATI
PORTE DI OUTPUT
DATA BUS


CPU
MEMORIA
IN
OUT
CPU
MEMORIA
IN
OUT
BUS DI
CONTROLLO



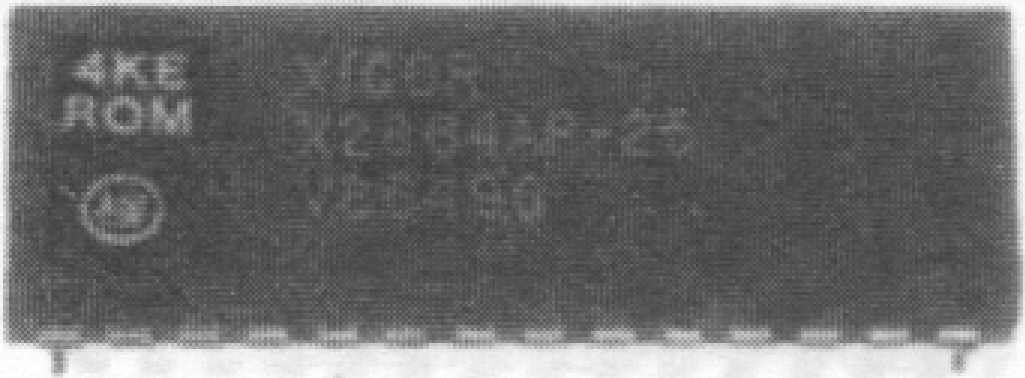
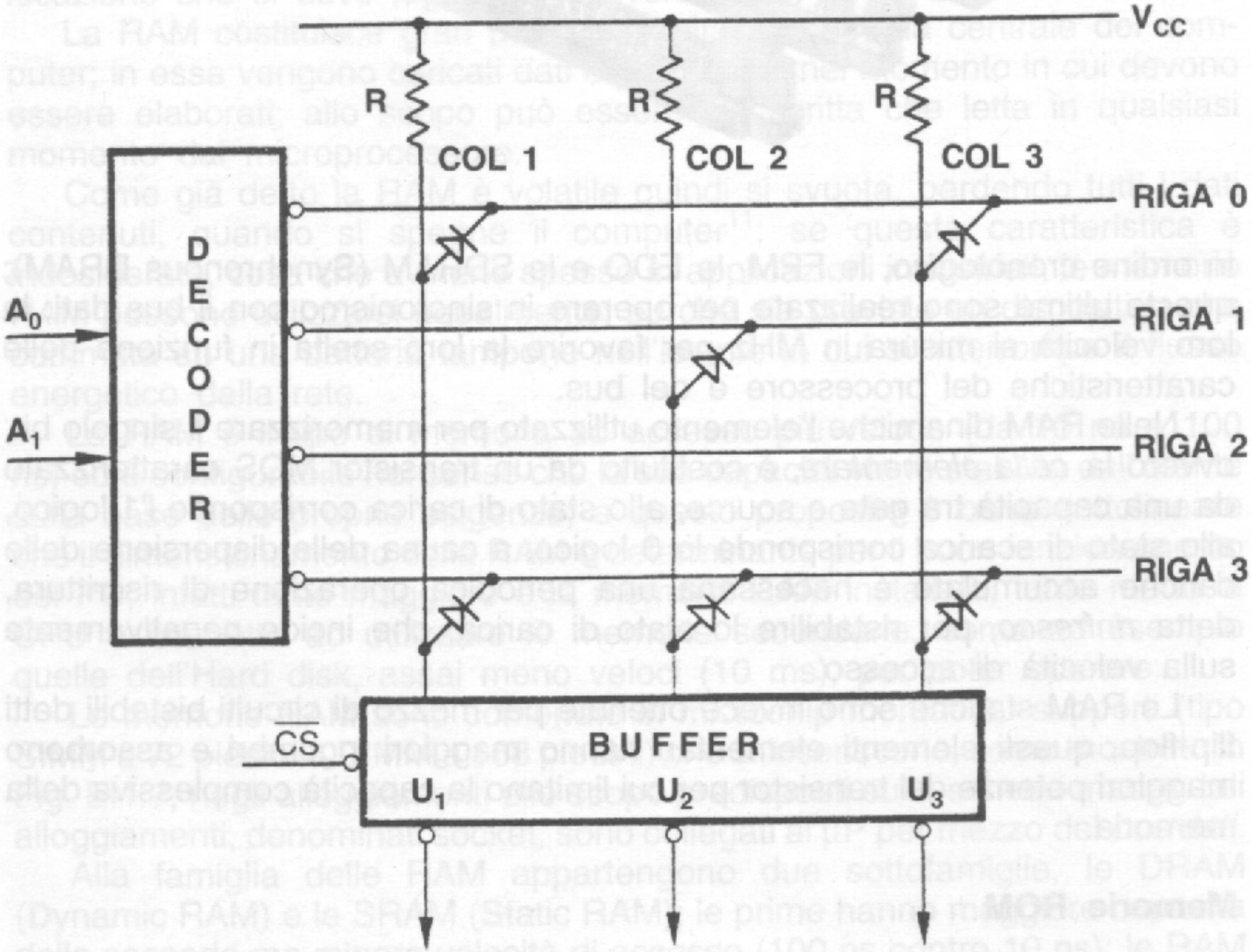


Fig. EI1.8 - Chip di memoria ROM.


V_{CC}
R
R
R
COL 1
COL 2
COL 3
RIGA 0
RIGA 1
RIGA 2
RIGA 3
DECODER
A_0
A_1
$\overline{CS}$
BUFFER
U_1
U_2
U_3

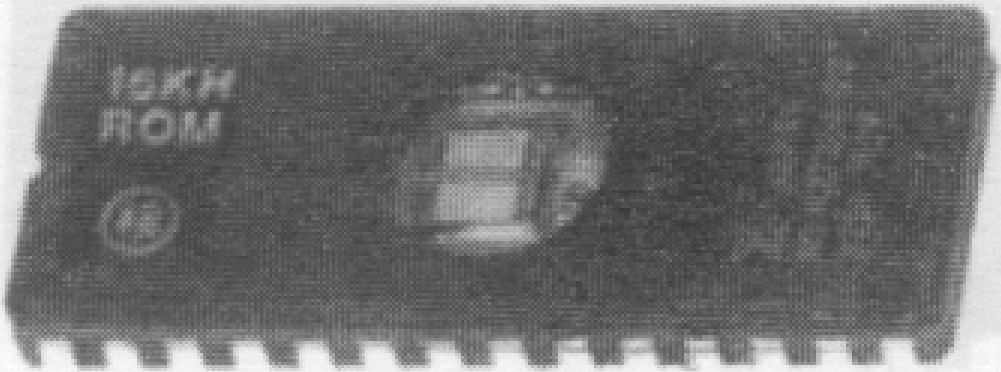
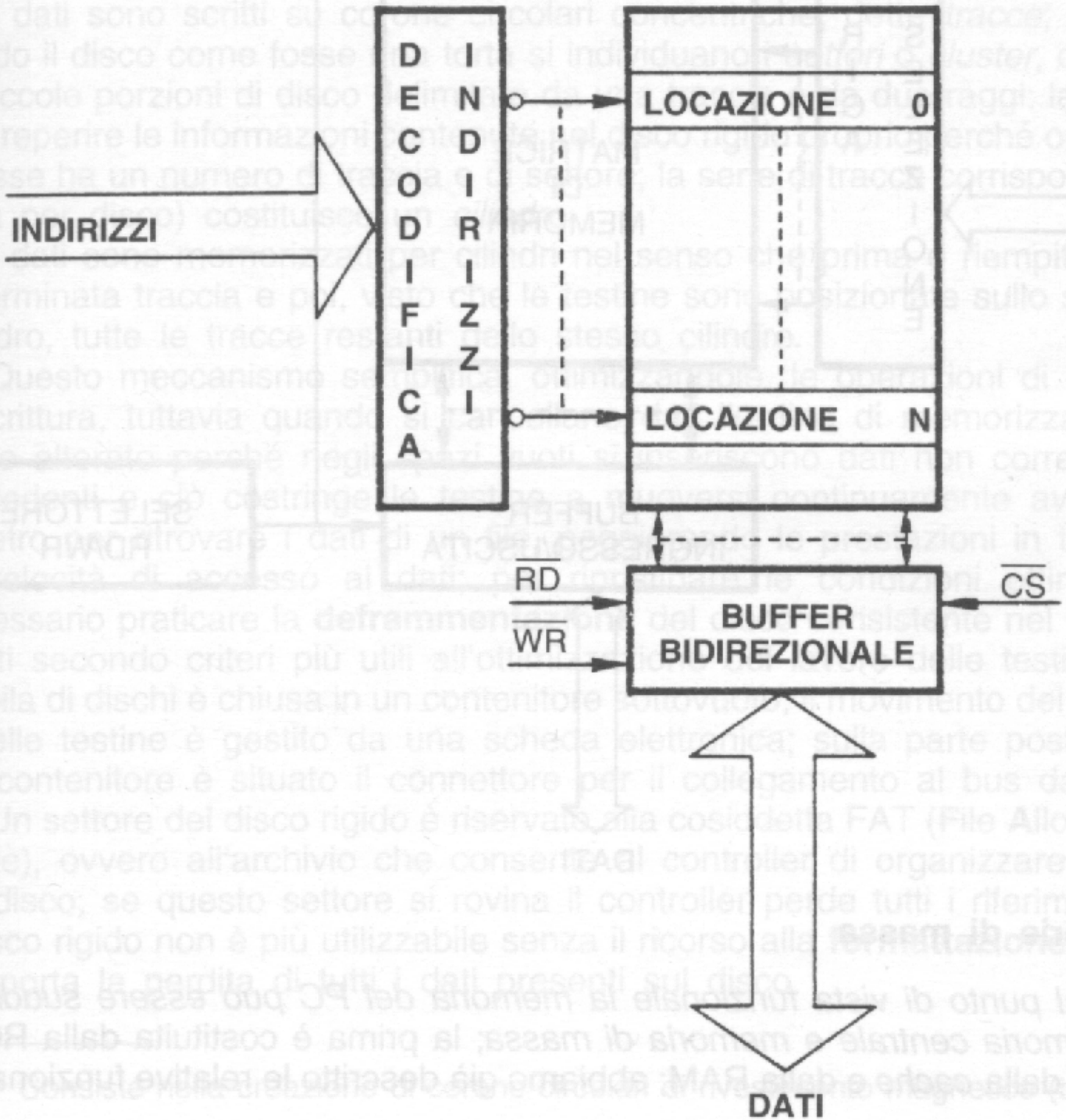
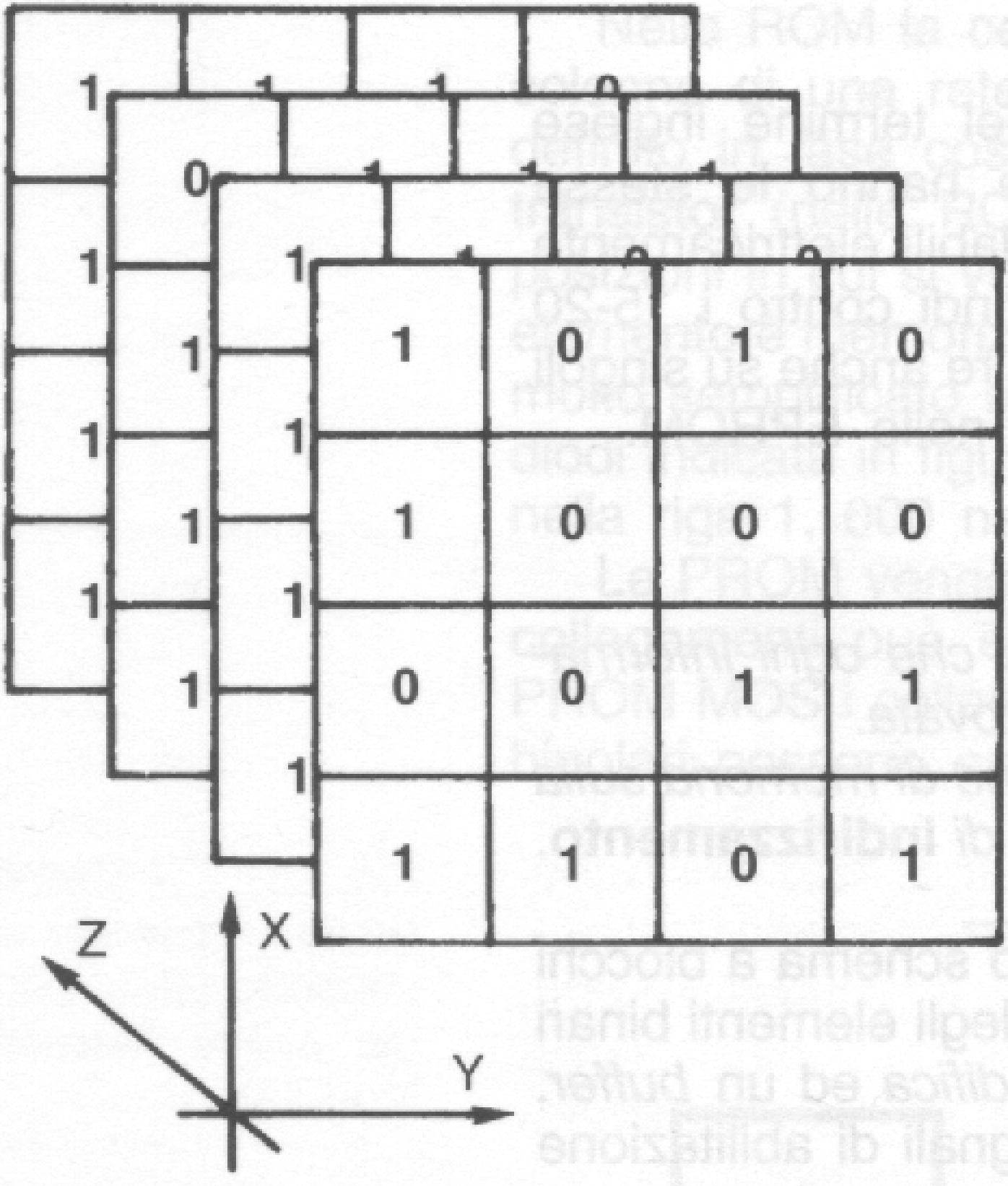


Fig. EI1.10 - Memoria EPROM.


INDIRIZZI
DECODIFICA INDIRIZZI
LOCAZIONE 0
LOCAZIONE N
RD
WR
CS
BUFFER BIDIREZIONALE
DATI


1 0 1 0
1 0 0 0
0 0 1 1
1 1 0 1
X
Z
Y

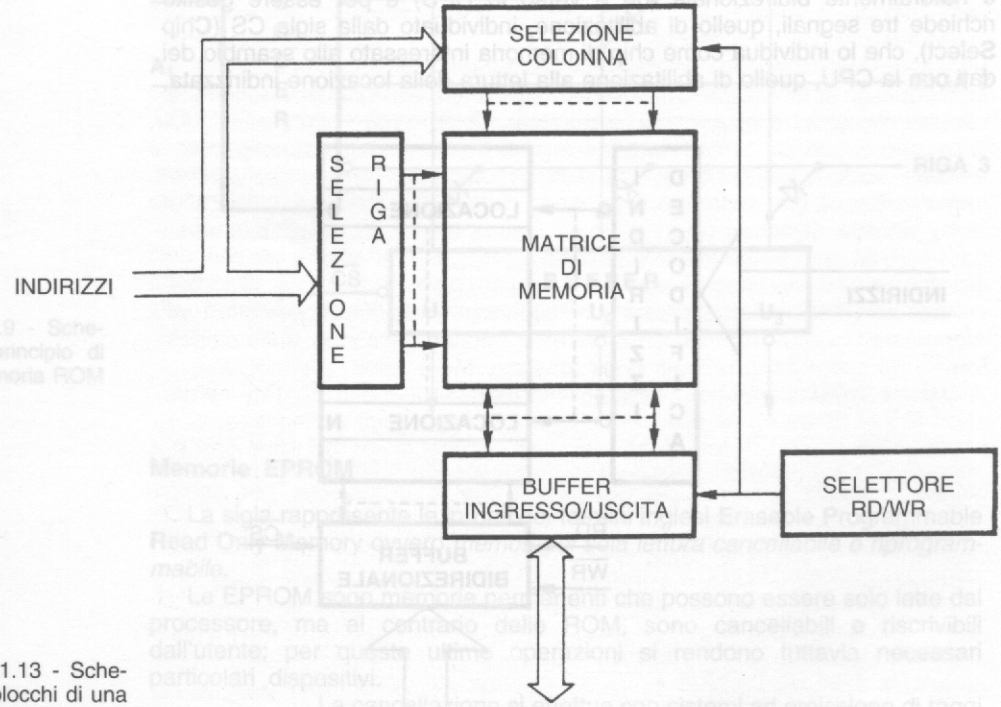


Fig. EI1.13 - Schema a blocchi di una RAM statica.

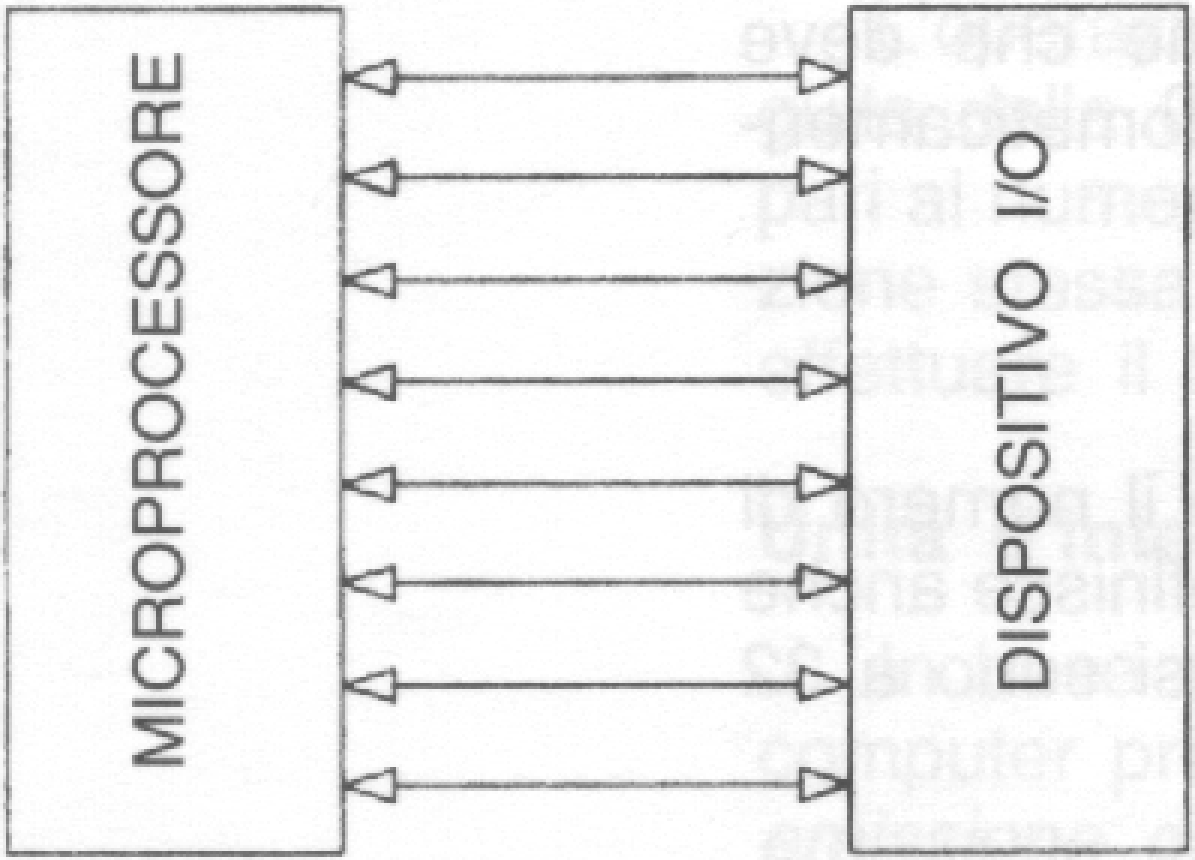
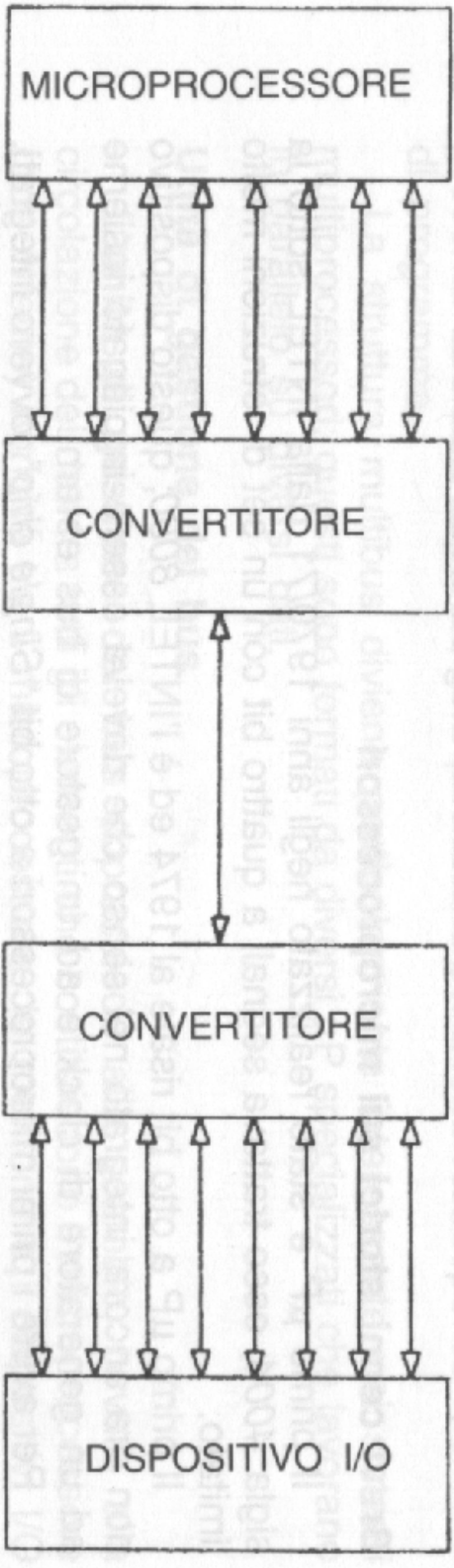


Fig.EI1.14 - Schema di collegamento di un dispositivo I/O parallelo.


MICROPROCESSORE
CONVERTITORE
CONVERTITORE
DISPOSITIVO I/O

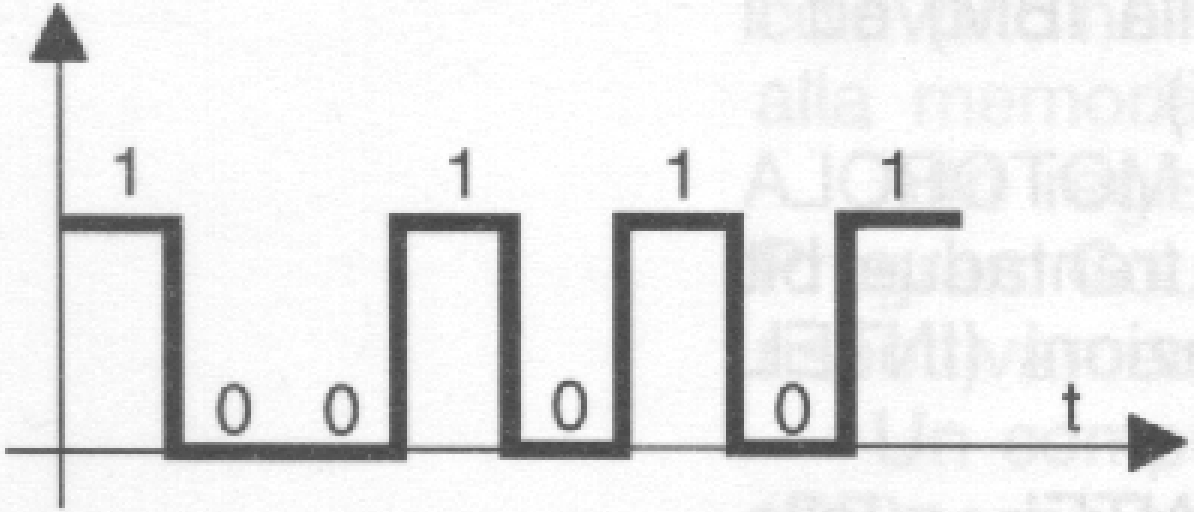
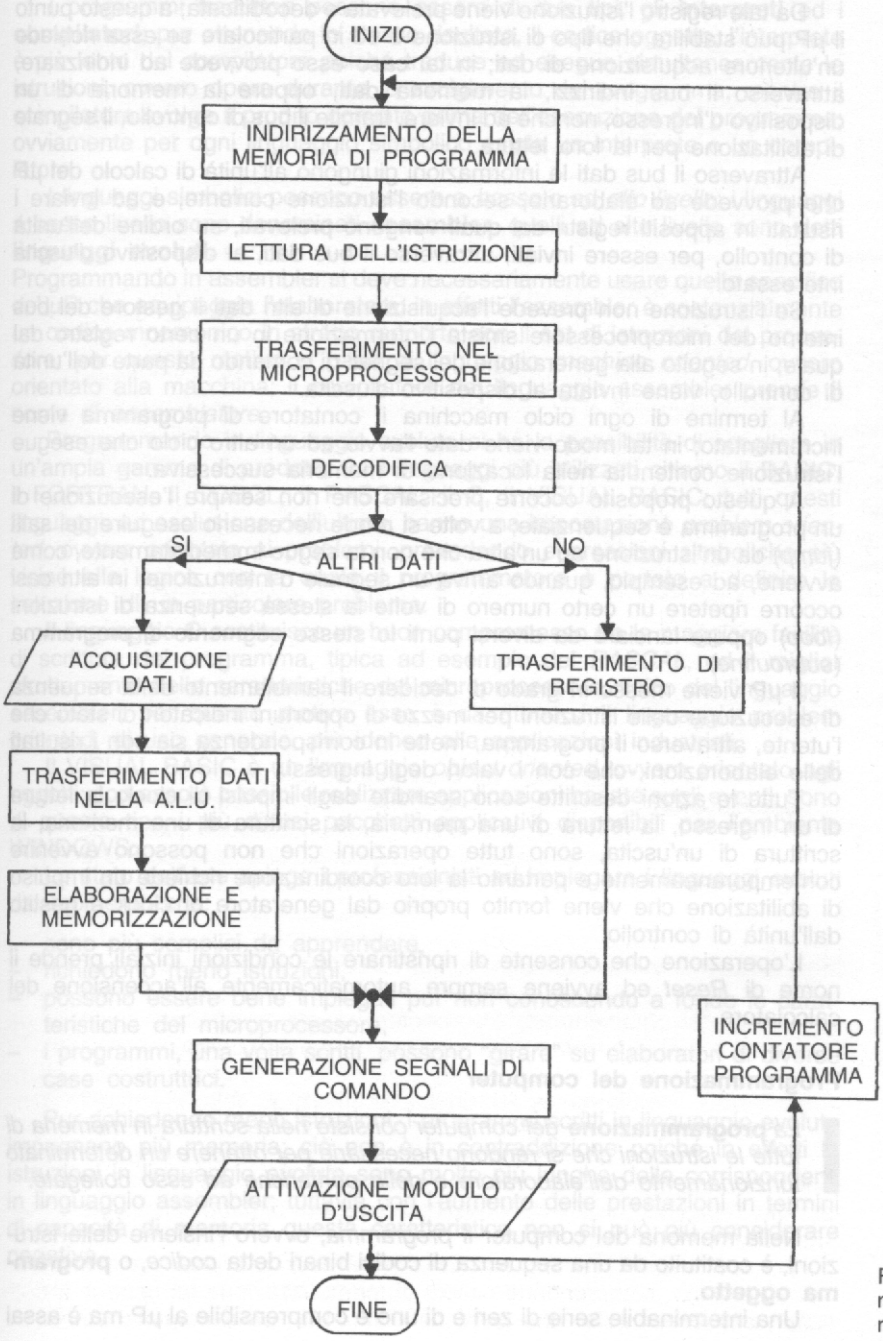


Fig. EI1.16 - Segnale di trasmissione seriale del dato 10010101.


INIZIO
INDIRIZZAMENTO DELLA MEMORIA DI PROGRAMMA
LETTURA DELL'ISTRUZIONE
TRASFERIMENTO NEL MICROPROCESSORE
DECODIFICA
ALTRI DATI
SI
NO
ACQUISIZIONE DATI
TRASFERIMENTO DATI NELLA A.L.U.
ELABORAZIONE E MEMORIZZAZIONE
TRASFERIMENTO DI REGISTRO
GENERAZIONE SEGNALI DI COMANDO
ATTIVAZIONE MODULO D'USCITA
INCREMENTO CONTATORE PROGRAMMA
FINE